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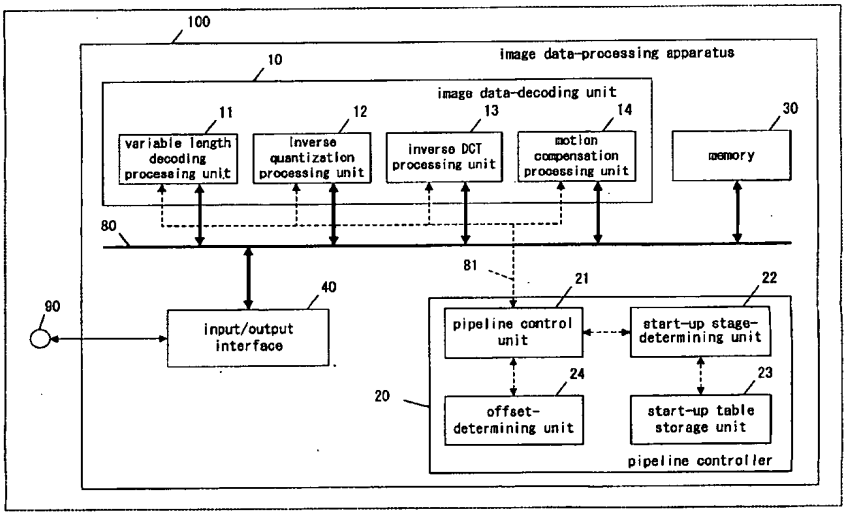
(54) Title: PIPELINE ARCHITECTURE FOR VIDEO ENCODER AND DECODER



(57) Abstract: An image data-processing apparatus (100) includes an image data-decoding unit (10) operable to execute pipeline processing-assisted image decoding processing, a pipeline controller (20) operable to control pipeline processing in the image data-decoding unit (10), a memory (30), and an input/output interface (40). The pipeline controller (20) executes control over the pipeline processing on the basis of information on the start-up of pipeline stages. The information is stored in a start-up table storage unit (23). The present configuration makes it feasible to provide an image data-processing apparatus operable to suppress degradation in decoded images to a minimum degree when pipeline control is disturbed upon the occurrence of decoding errors during the decoding processing, whereby high-quality images are realized.

WO 2006/041018 A1